MENG LI

University of Texas at Austin ⋄ Austin, TX 78712
meng_li@utexas.edu

RESEARCH INTERESTS

Design-for-Security techniques for hardware supply chain protection

Hardware reliability evaluation, simulation, and mitigation

EDUCATION

University of Texas at Austin, TX *Sep. 2013 - Present*
Ph.D. candidate, Department of Electrical and Computer Engineering
Advisor: David Z. Pan
GPA: 4.0/4.0

Peking University, Beijing, China *Sep. 2009 - Jul. 2013*
B.S., School of Microelectronics
GPA: 3.86/4.00, major: 3.92/4.00
Rank: 5/64

EXPERIENCE

Arm Inc. May 2017 - Sep. 2017
Research Intern *San Jose, CA*

· PrivyNet: a flexible framework for privacy-preserving deep neural network training with a fine-grained privacy control

Arm Inc. May. 2016 - Sep. 2016
Research Intern *San Jose, CA*

· Cross-level monte carlo framework for system vulnerability evaluation against fault attack

Cadence Design System May. 2014 - Aug. 2014
Research & Design Intern *Austin, TX*

· Fast timing analysis

ECE Department, University of Texas at Austin Aug. 2013 - Present
Graduate Student *Austin, TX*

· A practical split manufacturing framework for Trojan prevention via simultaneous wire lifting and cell insertion
· Provably secure camouflaging strategy for IC protection
· Practical public PUF enabled by solving max-flow problem on chip
· A Monte Carlo simulation flow for SEU analysis of sequential circuits

PUBLICATION

Preprint

[P1] **Meng Li**, Liangzhen Lai, Naveen Suda, Vikas Chandra, and David Z. Pan, "PrivyNet: A Flexible Framework for Privacy-Preserving Deep Neural Network Training with A Fine-Grained Privacy Control", arXiv preprint arXiv:1709.06161 (2017)

Journal Papers

[J6] Yibo Lin, Bei Yu, **Meng Li**, and David Z. Pan, "Layout Synthesis for Topological Quantum Circuits with 1D and 2D Architectures", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J5] **Meng Li**, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin and David Z. Pan, "Provably Secure Camouflaging Strategy for IC Protection", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J4] Jin Miao, *Meng Li*, Subhendu Roy, Yuzhe Ma and, Bei Yu, "SD-PUF: Spliced Digital Physical Unclonable Function", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J3] Xiaoqing Xu, Yibo Lin, **Meng Li**, Tetsuaki Matsunawa, Shigeki Nojima, Chikaaki Kodama, Toshiya Kotani, and David Z. Pan, "Sub-Resolution Assist Feature Generation with Supervised Data Learning", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2017 (accepted)

[J2] Xiaoqing Xu, Yibo Lin, **Meng Li**, Jiaojiao Ou, Brian Cline, and David Z. Pan, "Redundant Local-Loop Insertion for Unidirectional Routing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 7, pp. 1113-1125, July 2017

[J1] **Meng Li**, Runsheng Wang, Jibin Zou, and Ru Huang, "Characterization of Random Telegraph Noise in Scaled High-k/Metal-Gate MOSFETs with SiO2/HfO2 Gate Dielectrics", ECS Transactions, vol. 52, issue 1, pp. 941-946, 2013

Conference Papers

[C17] Che-Lun Hsu, Shaofeng Guo, Yibo Lin, Xiaoqing Xu, **Meng Li**, Runsheng Wang, Ru Huang, and David Z. Pan, "Layout-Dependent Aging Mitigation for Critical Path Timing", *Asia and South Pacific Design Automation Conference (ASPDAC)*, Jeju Island, Korea, Jan. 22-25, 2018

[C16] **Meng Li**, Bei Yu, Yibo Lin, Xiaoqing Xu, Wuxi Li, and David Z. Pan, "A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion", *Asia and South Pacific Design Automation Conference (ASPDAC)*, Jeju Island, Korea, Jan. 22-25, 2018

[C15] Wuxi Li, **Meng Li**, Jiajun Wang, and David Z. Pan, "UTPlaceF 3.0: A Parallelization Framework for Modern FPGA Global Placement", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Irvine, CA, Nov. 13-16, 2017 (Invited)

[C14] **Meng Li**, Liangzhen Lai, Vikas Chandra, and David Z. Pan, "Cross-level Monte Carlo Framework for System Vulnerability Evaluation against Fault Attack", *IEEE/ACM Design Automation Conference (DAC)*, Austin, TX, Jun. 18-22, 2017

[C13] Kaveh Shamsi, **Meng Li**, Travis Meade, Zheng Zhao, David Z. Pan, and Yier Jin, "Circuit Obfuscation and Oracle-guided Attacks: Who Can Prevail?", *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Banff, Alberta, Canada, May 10-12, 2017 (Invited)

[C12] Kaveh Shamsi, **Meng Li**, Travis Meade, Zheng Zhao, David Z. Pan, and Yier Jin, "Cyclic Obfuscation for Creating SAT-Unresolvable Circuits", *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Banff, Alberta, Canada, May 10-12, 2017

[C11] Kaveh Shamsi, **Meng Li**, Travis Meade, Zheng Zhao, David Z. Pan, and Yier Jin, "AppSAT: Approximately Deobfuscating Integrated Circuits", *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, McLean, VA, May 1-4, 2017 (Best Paper Award)

[C10] **Meng Li**, Kaveh Shamsi, Travis Meade, Zheng Zhao, Bei Yu, Yier Jin and David Z. Pan, "Provably Secure Camouflaging Strategy for IC Protection", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C9] Jin Miao, **Meng Li**, Subhendu Roy and Bei Yu, "LRR-DPUF: Learning Resilient and Reliable Digital Physical Unclonable Function", *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Austin, TX, Nov. 7-10, 2016

[C8] Shuang Song, **Meng Li**, Xinnian Zheng, Jee Ho Ryoo, Reena Panda, Michael LeBeane, Andreas Gerstlauer and Lizy K. John, "Proxy-Guided Load Balancing of Graph Processing Workloads on Heterogeneous Clusters", *IEEE International Conference on Parallel Processing (ICPP)*, Philadelphia, PA, Aug. 16-19, 2016

[C7] **Meng Li**, Ye Wang, and Michael Orshansky, "A Monte Carlo Simulation Flow for SEU Analysis of Sequential Circuits", *IEEE/ACM Design Automation Conference (DAC)*, Austin, TX, Jun. 5-9, 2016

[C6] **Meng Li**, Jin Miao, Kai Zhong, and David Z. Pan, "Practical Public PUF Enabled by Solving Max-Flow Problem on Chip", *IEEE/ACM Design Automation Conference (DAC)*, Austin, TX, Jun. 5-9, 2016

[C5] Xiaodan Xi, **Meng Li**, Jaeyoung Park, and Michael Orshansky, "Design Optimization of a Strong PUF Based on Nonlinearity of MOSFET Subthreshold Operation", *SRC Techcon*, Austin, TX, Sept. 20-22, 2015

[C4] Ye Wang, **Meng Li**, Xinyang Yi, Zhao Song, Michael Orshansky and Constantine Caramanis, "Novel Power Grid Reduction Method based on L1 Regularization", *IEEE/ACM Design Automation Conference (DAC)*, San Francisco, CA, Jun. 7-11, 2015

[C3] **Meng Li**, Yuan Yi, Derek Chiou, and Michael Orshansky, "An End-to-End SEU Simulation Platform", *SRC Techcon*, Austin, Tx, Sept. 20-22, 2014

[C2] Pengpeng Ren, Changze Liu, Runsheng Wang, **Meng Li**, Yangyuan Wang, and Ru Huang, "Impact of Cycle-to-Cycle Variation Effects on the Prediction of NBTI Degradation and the Resulted Dynamic Variations in high-k MOSFETs", *International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 22-24, 2013

[C1] Xiaobo Jiang, **Meng Li**, Runsheng Wang, Jiang Chen and Ru Huang, "Investigation on the Correlation Between Line-Edge-Roughness (LER) and Line-Width-Roughness (LWR) in Nanoscale CMOS Technology", *International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Xian, Shanxi, Oct.29 - Nov. 1, 2012

COURSES

VLSI I	Prof. Michael Orshansky
Computer Architecture	Prof. Aater Suleman
Optimization Issues in VLSI CAD	Prof. David Pan
Verification of Digital Systems	Dr. Jay Bhadra
Security HW/SW Interface	Dr. Mohit Tiwari
Embedded System Design/Modeling	Dr. Andreas Gerslauer
Probability & Stochastic Process I	Dr. Sanjay Shakkottai
Large Scale Optimization	Dr. Constatine Caramanis
Information Theory	Dr. Alexandros Dimakis
Monte Carlo Methods in Statistics	Dr. Peter Mueller
Numerical Linear Algebra	Dr. George Biros

SKILLS

Programming Languages
C/C++, Perl, Python (Tensorflow, Keras), Verilog

EDA Tools
Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler, Synopsys PrimeTime

HONORS AND AWARDS

Best paper award	HOST	2017
Cockrell School Graduate Student Fellowship	University of Texas at Austin	2013
Pacemaker to Merit Student	Peking University	2012
Merit Student	Peking University	2012
Yang Fuqing and Wang Yangyuan Academician Scholarship	Peking University	2011
Li Yanhong Baidu Scholarship	Peking University	2010